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METHOD FOR REDUCING LINE EDGE ROUGHNESS OF OXIDE MATERIAL USING CHEMICAL OXIDE REMOVAL

Abstract

A method for reducing line edge roughness (LER) of a semiconductor gate structure includes patterning a photoresist layer formed over an oxide hardmask layer. The photoresist layer is etched so as to transfer a photoresist pattern to the oxide hardmask layer, the photoresist pattern having an initial LER. The exposed surfaces of the oxide hardmask are etched with a chemical oxide removal (COR) so as to form a reaction product on the exposed surfaces, wherein concave portions of the exposed surfaces are etched at a reduced rate with respect to convex portions of the exposed surfaces.